RUMP SESSIONS
Tapa III, Honolulu I, II

Wednesday, June 16, 8:00 p.m. – 10:00 p.m.
Co-Chairs: M-R. Lin, AMD
K. Sakamoto, AIST

RJ1 What's Beyond the Planar MOSFET?
Tapa I
Organizers:

Circuits	**Technology**
K. Bernstein, IBM	M-R. Lin, AMD
K. Mashiko, STARC	Y. Omura, Kansai Univ

Moderator: J. Graham, Hewlett Packard
K. Saraswat, Stanford Univ.

The ability to extend the Field Effect Transistor's electrical scaling and on-chip device count beyond the 65 nm lithography node requires reduction in device static leakage currents. Multiple mechanisms now contribute to the overall static power loss. A number of novel non-planar device structure and material remedies have recently been proposed. Each of these approaches, however, introduces new idiosyncrasies and challenges that circuit designers, device/process engineers, and EDA developers would have to accommodate. Our panel of experts on these specific solutions will briefly explain their individual views of the future and the subset of problems their approaches will assert. Our audience of expert technology developers and product designers will have the opportunity to challenge their conclusions and judge which of the scenarios is most likely to resemble the future direction for our industry.

Panelists

G. Bernstein, Notre Dame Univ.
R. Chau, Intel
Y. Hagiwara, Sony
Y. Nishi, Stanford
L. Scheffer, Cadence
H-S Philip Wong, IBM
K. Yano, Hitachi

R2 Is DRAM Dead? Will Flash Rule the World?
Honolulu I
Moderators: G. Atwood, Intel
K. Kim, Samsung

DRAM is the long established technology and product leader for silicon memory development driven primarily by its use in personal computers. Today it is the largest consumer of silicon of any of the memory technologies and defines the roadmap for silicon memory scaling and advanced processing tool development.

Flash memory has seen explosive growth over the past several years due to the emergence of portable consumer devices such as cell phones, cameras, and music players. For these devices, Flash is serving as the storage for code with the device directly executing from the Flash memory instead of DRAM, as well as the storage for data with the Flash serving as a solid state disk.

Flash memories have, to date, largely drafted off of DRAM or Logic technologies adding incremental development for Flash specific functionality. Projections indicate that Flash will exceed DRAM for the number of bits shipped in the near future, becoming the dominate memory technology.

This panel will attempt to answer the questions:

Will Flash change the memory subsystem, reducing the value of DRAM? Are portable applications changing the memory requirements in favor of Flash? Is Flash more scalable than DRAM, thus better suited to drive technology? Will the Flash cost structure and features change the balance of volatile vs. non-volatile memory in the system? Will Flash replace DRAM as the memory technology driver?

Panelists:

J. Alsmeier, Infineon Technologies
G. Casagrande, STMicroelectronics
C-H Kim, Samsung Elec.
L. Tran, Micron Technology, Inc.
K. Sato, Elpida Memory Inc.
R. Shirota, Toshiba Corp.

R3 Strained Si for Enhanced CMOS Performance
Honolulu II
Moderators: D. Antoniadis, Massachusetts Institute of Technology
S. Takagi, University of Tokyo

With the advent of the 90 nm CMOS node many large manufacturers are introducing some form of stress to the silicon substrate at the MOSFET channel area in order to enhance carrier mobility and therefore current drive. The most common scheme appears to be localized strain produced by stressor films or other localized processes, and various current boosts are claimed. On the other hand, most of the pioneering and best documented work with strained silicon has utilized uniform Si/SiGe substrates with global biaxial strain. This rump session will review various methods for channel straining, will address the pros and cons of those methods from the viewpoint of device engineering and wafer manufacturing, and will examine potential strained channel roadmaps.

Panelists:

K. Goto, Fujitsu
J. Hoyt, Massachusetts Inst. of Technology
M. Ieong, IBM
S. Kimura, Hitachi
A. Lochtefeld, Amberwave
K. Mistry, Intel
M. Nakamae, SUMC